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10/075,868	02/13/2002	Josef Schmid	3	9427

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Docket Administrator (Room 3J-219)
Lucent Technologies Inc.
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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,868	SCHMID, JOSEF	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL DETAILED ACTION

1. Claims 1-21 have been canceled and claims 22-28 have been added. Claims 22-28 have been examined. The proposed changes to the drawing are accepted by the Examiner.

2. The objections to the claims and drawings and rejections under 35 U.S.C. 112 of record are withdrawn in response to Applicant's amendment.

3. Applicant's arguments with respect to claims 22-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 22, 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22:

a. The recited claim limitation "entering a delay measurement mode" and "performing a delay measurement" is vague and indefinite. The claim does not disclose ant conditions on how the delay measurement conducted. Although the

claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

b. The recited claim limitation "the combinational circuit does not interfere with the operation of the scan chain due to the delay chain output port being keep in tristate condition or by pulling the test data input to operating voltage" is vague and indefinite. It is not clear to the Examiner during what mode these conditions exist. Also, it is not clear what "pulling the test data input to operating voltage" means. Changing the condition on the TDI input does not change the tristate condition of the boundary scan buffer. Clarification of the claim language is required.

Claim 25:

This claim recites the limitation "the at least one boundary scan cell" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 26:

This claim recites the limitation "said respective two scan ports" in line 3. There is insufficient antecedent basis for this limitation in the claim. It's not clear to the Examiner which scan ports this limitation is referring to, i.e. SI, SO, DCO. Clarification is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al. (US-6314539), hereinafter Jacobson, in view of Whetsel (5710779), hereinafter Whetsel.

Claim 22:

Jacobson teaches BSR cell 800 includes a test data input (TDI) terminal (SI), a SYSTEM DATA IN terminal, an input multiplexer (MUX) 810, a shift register flip-flop 820 (a storage layer between a scan input port (SI) and a scan output port (SO)), a test data output (TDO) terminal (SO), a parallel latch 830, an output MUX 840 and a SYSTEM DATA OUT terminal. (Col. 9, lines 59-63). Jacobson also teaches bypass MUX 850 includes a first input terminal connected to the TDI terminal, a second input terminal connected to the output terminal of shift register flip-flop 820, and an output terminal connected to the TDO terminal that is used to shift data signals along the BSR. Jacobson further teaches when select control circuit 855 transmits a second (e.g., low) signal (**the combinational circuit does not interfere with the operation of the scan chain ...**), bypass MUX 850 passes signals directly from the TDI terminal, thereby bypassing input MUX 810 and shift register flip-flop 820, effectively by programming bypass MUX 850 to pass data signals directly from the TDI terminal to the TDO terminal

(creating an additional combinational path (BP) between the scan input port (SI) and a scan output port (SO)). (Col. 10, lines 15-29). Jacobson does not explicitly teach connecting the output port (SO) of a boundary scan cell forming the end of the scan chain to a separate delay chain output port (DCO). However, Jacobson does teach that the PLD 1100 is configured to perform Boundary-Scan Test procedures where BSR cells that are used by neither first logic function 1118(A) nor second logic function 1118(B) are effectively removed from the BSR by programming the bypass circuits of these BSR cells to pass signals directly from their TDI terminals to their TDO terminals (**delay measurements of an integrated circuit having a scan chain for boundary scan testing**). (Col. 13, lines 22-29, FIG. 11A). Whetsel teaches the use of an additional test output pin (or terminal) TO is added to the IC to output data (**a separate delay chain output port (DCO) ... which is additional to the test data output port**) during observation and bypass modes of a selected scan path where the TO pin is 3-state (**delay chain output port being keep in tristate condition**) so that multiple ICs can have a bussed TO connection at the board level. (Col. 5, 26-31, FIG. 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's TDO output to add Whetsel's test output pin (or terminal) TO. The artisan would have been motivated to do so because the additional test output terminal TO would enable Jacobson to control the delay chain output with the 3-state buffer.

Claim 23:

Jacobson teaches the variable length BSR of PLD 1100 has an effective length of 10 BSR cells, which is less than half of the maximum length (27 BSR cells) of the

BSR where the reduced-length BSR facilitates significantly faster Boundary-Scan Test procedures (**performing the delay measurement at the test output port (TDO) for boundary scan testability**) over conventional fixed-length BSRs because significantly less data is required. (Col. 13, lines 22-51, FIG. 11A).

Claim 24:

Jacobson teaches BSR cell 800 includes a test data input (TDI) terminal (SI), a SYSTEM DATA IN terminal, an input multiplexer (MUX) 810, a shift register flip-flop 820 (a storage layer between a scan input port (SI) and a scan output port (SO)), a test data output (TDO) terminal (SO), a parallel latch 830, an output MUX 840 and a SYSTEM DATA OUT terminal (**scan cells forming the scan chain have a storage layer between a scan input port and an output port**). (Col. 9, lines 59-63). Jacobson also teaches bypass MUX 850 (**a multiplexer, connected to the output of the additional combinational path...**) includes a first input terminal connected to the TDI terminal (**an additional combinational path...**), a second input terminal connected to the output terminal of shift register flip-flop 820, and an output terminal connected to the TDO terminal that is used to shift data signals along the BSR. (Col. 10, lines 15-19). Jacobson further teaches a PLD 1100 that is configured to perform Boundary-Scan Test procedures where BSR cells that are used by neither first logic function 1118(A) nor second logic function 1118(B) are effectively removed from the BSR by programming the bypass circuits of these BSR cells to pass signals directly from their TDI terminals to their TDO terminals (**connecting the scan input port (SI) of a first scan cell to a test data input port (TDI) for boundary scan testing and the scan output port (SO) of a**

scan cell forming the end of the scan chain via a test data output path to a test data output port (TDO) for boundary scan testing). (Col. 13, lines 22-29, FIG. 11A). Jacobson does not explicitly teach connecting the output port (SO) of a boundary scan cell forming the end of the scan chain to a separate delay chain output port (DCO). However, Jacobson does teach that the PLD 1100 is configured to perform Boundary-Scan Test procedures where BSR cells that are used by neither first logic function 1118(A) nor second logic function 1118(B) are effectively removed from the BSR by programming the bypass circuits of these BSR cells to pass signals directly from their TDI terminals to their TDO terminals (**output port of a boundary scan cell forming the end of the scan chain**). (Col. 13, lines 22-29, FIG. 11A). Whetsel teaches the use of an additional test output pin (or terminal) TO is added to the IC to output data (**the separate delay chain output port (DCO)**) during observation and bypass modes of a selected scan path where the TO pin is 3-state so that multiple ICs can have a bussed TO connection at the board level. (Col. 5, 26-31, FIG. 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's TDO output to add Whetsel's test output pin (or terminal) TO. The artisan would have been motivated to do so because the additional test output terminal TO would enable Jacobson to control the delay chain output with the 3-state buffer.

Claim 25:

"providing of the at least one boundary scan cell according to the IEEE Standard 1149.1"

Jacobson teaches in FIG. 2 a detailed block diagram showing an example of the basic hardware elements provided on an IEEE Standard 1149.1 compliant PLD where the basic hardware elements include a test access port (TAP) 210, a TAP controller 220, an instruction register (IR) 230, an instruction decode circuit 235, a test data register circuit 240, an output multiplexer (MUX) 250, an output flip-flop 260 and a tri-state buffer 270. Jacobson also teaches TAP 210 provides access to the test support functions build into an IEEE Standard 1149.1 compliant PLD and includes three input connections for receiving the test clock input (TCK) signal, the test mode select (TMS) signal, and the test data input (TDI) signal (providing of the at least one boundary scan cell according to the IEEE Standard 1149.1). (Col. 3, lines 43-61).

Claim 26:

Jacobson teaches bypass MUX 850 includes a first input terminal connected to the TDI terminal, a second input terminal connected to the output terminal of shift register flip-flop 820, and an output terminal connected to the TDO terminal that is used to shift data signals along the BSR. Jacobson also teaches when select control circuit 855 transmits a second (e.g., low) signal, bypass MUX 850 passes signals directly from the TDI terminal, thereby bypassing input MUX 810 and shift register flip-flop 820, effectively by programming bypass MUX 850 to pass data signals directly from the TDI terminal (SI) to the TDO terminal (SO) (**implementing a local path between said respective two scan ports...**) by bypassing the respective storage layer of a boundary scan cell). (Col. 10, lines 15-29).

Claim 27:

Jacobson teaches bypass MUX 850 includes a first input terminal connected to the TDI terminal, a second input terminal connected to the output terminal of shift register flip-flop 820, and an output terminal connected to the TDO terminal that is used to shift data signals along the BSR. Jacobson also teaches when select control circuit 855 transmits a second (e.g., low) signal, bypass MUX 850 passes signals directly from the TDI terminal, thereby bypassing input MUX 810 and shift register flip-flop 820, effectively by programming bypass MUX 850 to pass data signals directly from the TDI terminal to the TDO terminal (**combinational path is connected to the scan output port via a multiplexer controlled by the shift signal from a test access port controller**). (Col. 10, lines 15-29).

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al. (US-6314539), hereinafter Jacobson, in view of Whetsel (5710779), hereinafter Whetsel in further view of Abadir et al. (US-2002/0112213), hereinafter Abadir.

Claim 28:

Jacobson does not explicitly teach "**the combinational path (BP) is defined as a false path during synthesizing of the scan chain**". Abadir teaches a design analysis tool and method of use for false timing path identification for industrial circuits, both on the integrated circuit (IC) scale as well as a board level. (Page 4, ¶21). It would have been obvious to one of ordinary skill in the art at the time the invention was made use Abadir's design analysis tool and method to synthesize Jacobson's boundary scan

circuit to set false path information for the combinational path (BP). The artisan would have been motivated to do so because, as a result of Abadir's design analysis tool and method, engineering resources could be preserved by minimizing wasteful efforts spent on optimizing false timing paths. Furthermore, the artisan would have been motivated to do so because Abadir's design analysis tool and method eliminates the creation of unnecessary circuit area, the dissipation of additional power, and reduction in performance which is typically associated with the optimization of false paths.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

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